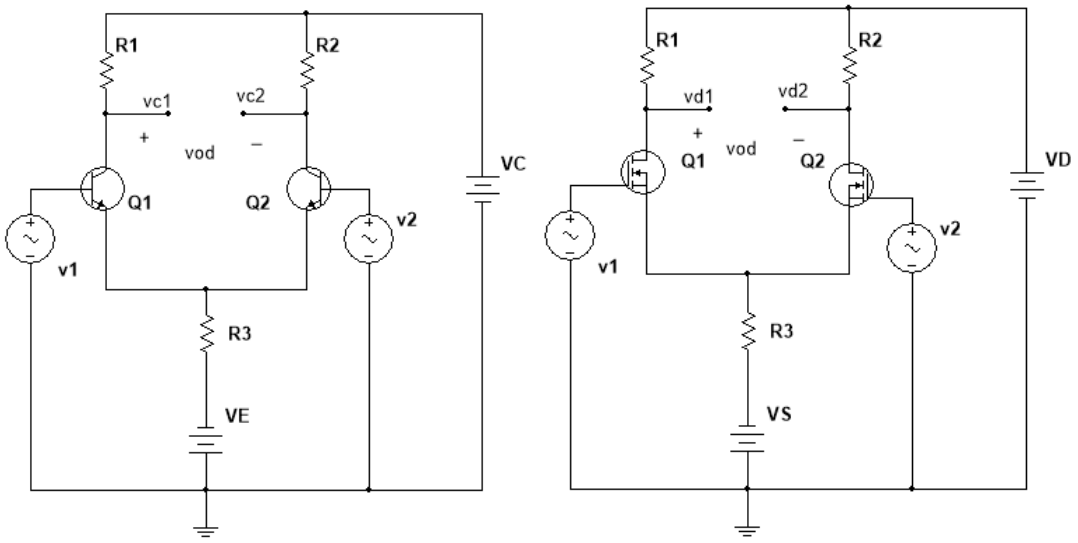
Chapter 8

Differential Amplifier
Operational Amplifier Design

1) Fundamentals of the Basic Configuration

As we see from the figures below, the basic configuration of a differential amplifier is the utilization of two **matched** transistors having their emitters or sources connected, the inputs applied through their bases or gates, and the outputs taken at the collectors or drains. Note that we are using mainly NPN BJT transistors or NMOS enhanced-mode FETs. To achieve transistors with similar properties, they should be fabricated on the same wafer at a given time (integrated circuits)



Let us define some useful entities that will assist us in the analysis of these configurations. In this particular case, the differential input and the common-mode input will, respectively, be defined as:

$$v_{id} = v_1 - v_2$$

$$v_{ic} = (v_1 + v_2)/2$$

Similarly, one can show that

$$v_1 = v_{ic} + v_{id}/2$$

$$v_2 = v_{ic} - v_{id}/2$$

However, you may elect to define $v_{id} = v_2 - v_1$ if you so desire. In this analysis, we will use the first definition.

In addition, the differential output and the common-mode output will, respectively, be defined as:

- BJT $\mathbf{v_{od} = v_{c1} - v_{c2}}$ $\mathbf{v_{oc} = (v_{c1} + v_{c2})/2}$
- MOSFET $\mathbf{v_{od} = v_{d1} - v_{d2}}$ $\mathbf{v_{oc} = (v_{d1} + v_{d2})/2}$

It is evident that the other choice for v_{od} can be made.
Often, the subsequent stages have only one input, and in that case, the output of the differential pair is at one of the collectors or drains. The configuration will then be labeled a single-ended output differential pair.

2) DC Analysis

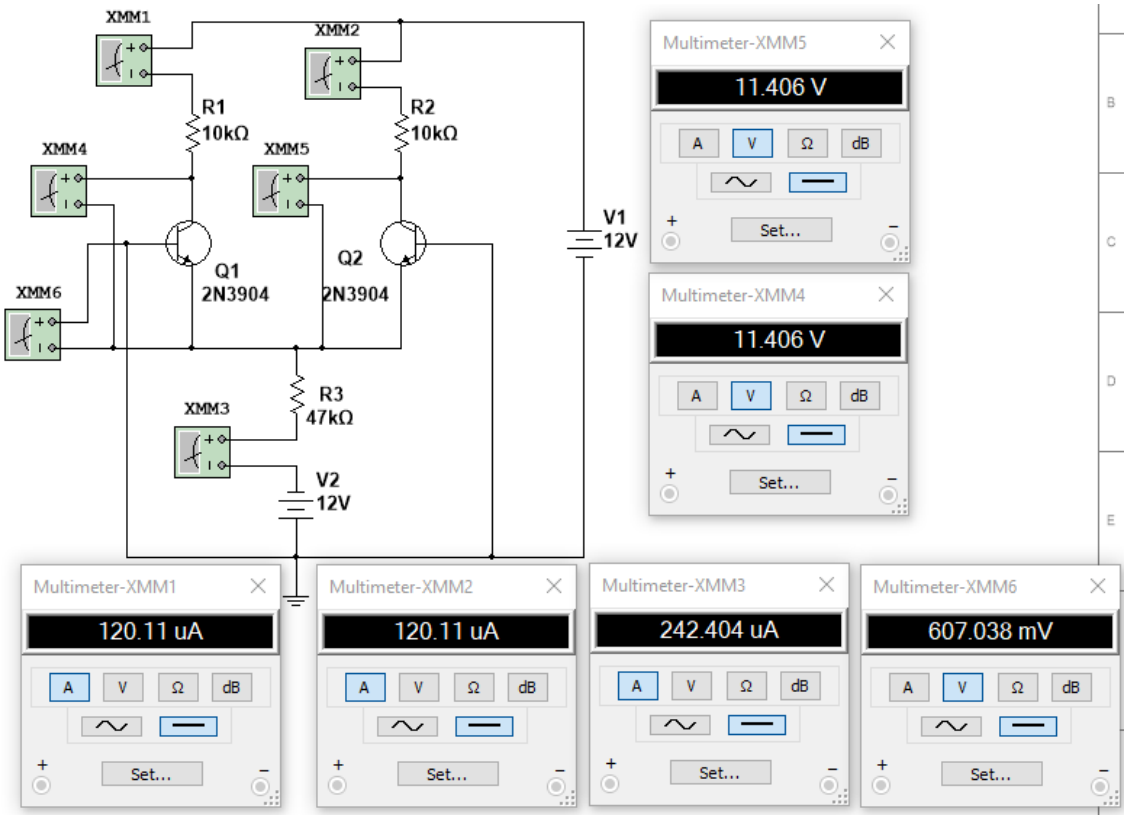
- BJT

Let us label our components as follows:

$$R_1 = R_2 = R_C$$
$$R_3 = R_{EE}$$
$$V_C = V_{CC}$$
$$V_E = V_{EE}$$

Since the transistors are matched, and considering the simplest relationship between the current I_C and the voltage V_{BE} ($I_C = I_S \exp(-V_{BE}/V_T)$), which in this case is the same for both transistors (bases connected to each other through ground, and the emitters connected to each other)

$$V_{BE1} = V_{BE2} = V_{BE}$$
$$I_{C1} = I_{C2} = I_C$$
$$I_{E1} = I_{E2} = I_E$$
$$I_{B1} = I_{B2} = I_B$$
$$V_{C1} = V_{C2} = V_{CC} - R_C I_C$$
$$V_{CE1} = V_{CE2} = V_{CE}$$
$$V_{OD} = V_{C1} - V_{C2} = 0V$$



Assume $V_{BEQ} = 0.7V$, Beta = 136

$R_{C1} = R_{C2} = R_C = R_1 = R_2 = 10k\Omega$

$R_{EE} = R_3 = 47k\Omega$

$V_{CC} = V_1 = 12V$

$V_{EE} = V_2 = 12V$

```
R1=10e3;R2=10e3;R3=47e3;
VBEQ=0.7;beta=136;V1=12;V2=12;
IEEQ=(V2-VBEQ)/R3;
IEQ=IEEQ/2;
ICQ=beta/(beta+1)*IEQ;
VCEQ=V1+VBEQ-R2*ICQ;
disp(['The Q-point is ICQ = ',num2str(ICQ*1000),' mA'])
disp([' VCEQ = ',num2str(VCEQ),' V'])
```

The Q-point is ICQ = 0.11934 mA

VCEQ = 11.5066 V

We can see that the results through calculations are very close to the ones obtained through Multisim.

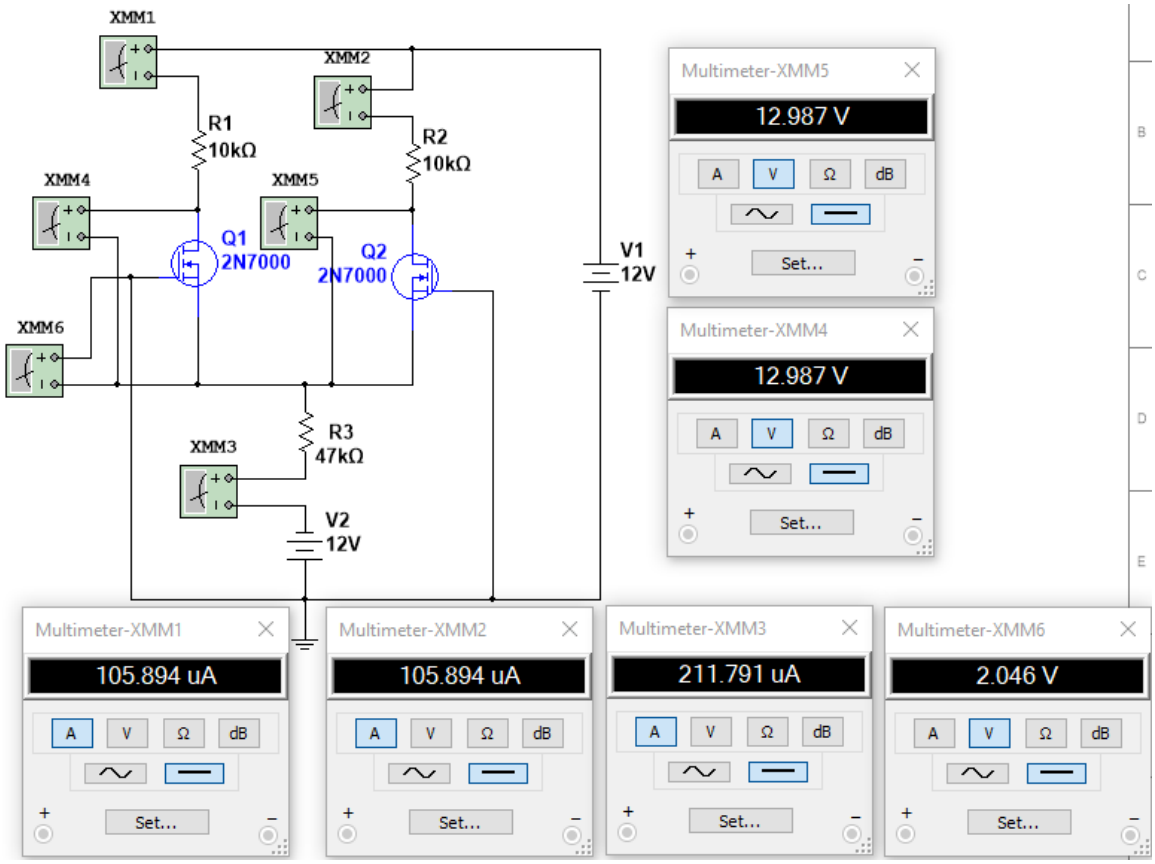
- MOSFET

We will follow the same model used for the BJT.
Let us label our components as follows:

$$R_D = R_1 = R_2$$
$$R_{SS} = R_3$$
$$V_{DD} = V_1$$
$$V_{SS} = V_2$$

Since the transistors are matched, and considering the simplest relationship between the current I_{DS} and the voltage V_{GS} ($I_{DS} = K_n/2\ (V_{GS} - V_{TN})^2$), which in this case is the same for both transistors (gates connected to each other through ground, and the sources connected to each other)

$$V_{GS1} = V_{GS2} = V_{GS}$$
$$I_{DS1} = I_{DS2} = I_{DS}$$
$$V_{D1} = V_{D2} = V_{DD} - R_D\ I_{DS}$$
$$V_{DS1} = V_{DS2} = V_{DS}$$
$$V_{OD} = V_{D1} - V_{D2} = 0V$$



Assume $V_{TN} = 2V$, $K_n = 0.1$

$R_{D1} = R_{D2} = R_D = R_1 = R_2 = 10k\Omega$

$R_{SS} = R_3 = 47k\Omega$

$V_{DD} = V_1 = 12V$

$V_{SS} = V_2 = 12V$

```
R1=10e3;R2=10e3;R3=47e3;V1=12;V2=12;Kn=0.1;VTN=2;
p=[4*R3^2, -(4*R3*(V2-VTN)+2/Kn),(V2-VTN)^2];
Ids=roots(p);
Vds=V1+V2-(R2+2*R3)*Ids;
Vgs=V2-2*R3*Ids;
disp(['The two possible values for Ids are      ',num2str(1000*Ids'), ' mA'])
disp(['The two possible values for Vds are      ',num2str(Vds'), ' V'])
disp(['The two possible values for Vgs are      ',num2str(Vgs'), ' V'])
for i=1:2
   if Vgs(i)>VTN
```

```
        disp(['The Q-point is IDSQ = ',num2str(Ids(i)*1000),' mA'])
        disp([' VDSQ = ',num2str(Vds(i)),' V'])
    end
end
```

The two possible values for Ids are 0.10687 0.10589 mA

The two possible values for Vds are 12.885 12.9871 V

The two possible values for Vgs are 1.9538 2.046 V

The Q-point is IDSQ = 0.10589 mA

VDSQ = 12.9871 V

We can see again that the results through calculations are very close to the ones obtained through Multisim. The minor variations may be due to the fact that we ignored the effect of V_{DS} on I_{DS} through lambda which is small in this case (lambda = 1.46e-4)

3) Linearity Requirements

- BJT

Remember the standard labeling

$x_Y = X_Y + x_y$

X_Y is the DC component (both variable and subscript are capital case)

x_y is the AC component (both variable and subscript are small case)

$i_{C1} = I_S\, e^{v_{BE1}/V_T}$

$i_{C2} = I_S\, e^{v_{BE2}/V_T}$

Assuming matched transistors,

$$\frac{i_{C2}}{i_{C1}} = \frac{I_S\, e^{v_{BE2}/V_T}}{I_S\, e^{v_{BE1}/V_T}} = e^{(v_{BE2}-v_{BE1})/V_T}$$

If the difference in base voltage is 58mV, one current is going to be 10 times larger than the other current (it will increase 10 fold for every 58mV increase in the base voltage. Of course, we are assuming V_T = 25mV at room temperature

Remember the standard labeling

$$i_{C1} = I_S\, e^{v_{BE1}/V_T}$$

$$i_{C2} = I_S\, e^{v_{BE2}/V_T}$$

Assuming matched transistors,

$$\frac{i_{C2}}{i_{C1}} = \frac{I_S\, e^{v_{BE2}/V_T}}{I_S\, e^{v_{BE1}/V_T}} = e^{(v_{BE2}-v_{BE1})/V_T}$$

$$\frac{i_{C1}-i_{C2}}{i_{C1}+i_{C2}} = \frac{e^{v_{BE1}/V_T} - e^{v_{BE2}/V_T}}{e^{v_{BE1}/V_T} + e^{v_{BE2}/V_T}}$$

$$\frac{e^a - e^b}{e^a + e^b} = \frac{e^b(e^{a-b}-1)}{e^b(e^{a-b}+1)} = \frac{e^{(a-b)/2}(e^{(a-b)/2} - e^{-(a-b)/2}1)}{e^{(a-b)/2}(e^{(a-b)/2} + e^{-(a-b)/2}1)} = \tanh((a-b)/2)$$

$$\frac{i_{C1}-i_{C2}}{i_{C1}+i_{C2}} = \tanh\left(\frac{v_{BE1}-v_{BE2}}{2V_T}\right)$$

Since $i_{E1} + i_{E2} = I_{EE}$

then $i_{C1} + i_{C2} = \alpha I_{EE}$

Hence

$$i_{C1} - i_{C2} = \alpha I_{EE} \tanh\left(\frac{v_{BE1}-v_{BE2}}{2V_T}\right)$$

$$i_{C1} - i_{C2} = \alpha 2I_E \tanh\left(\frac{v_{BE1}-v_{BE2}}{2V_T}\right)$$

$$i_{C1} - i_{C2} = 2I_C \tanh\left(\frac{v_{BE1}-v_{BE2}}{2V_T}\right) = 2I_C \tanh\left(\frac{v_{id}}{2V_T}\right)$$

because $v_{BE1} - v_{BE2} = (v_{be1} + V_{BE1}) - (v_{be2} + V_{BE2})$

and $V_{BE1} = V_{BE2}, v_{id} = v_1 - v_2$

$$i_{C1} - i_{C2} = 2I_C\left[\left(\frac{v_{id}}{2V_T}\right) - \frac{1}{3}\left(\frac{v_{id}}{2V_T}\right)^3 + \frac{2}{15}\left(\frac{v_{id}}{2V_T}\right)^5 - \frac{17}{315}\left(\frac{v_{id}}{2V_T}\right)^7 + \ldots\right]$$

If we assume the termss beyond the third degree term are negligible
and that the third degree term is less than 10% of the first degree term, hence negligible
and $i_{C1} - i_{C2} = i_{c1} - i_{c2}$ since $I_{C1} = I_{C2}$
Therefore i_{C1} - i_{C2} will be linearly related to v_{id} when

$$\frac{1}{3}\left(\frac{v_{id}}{2V_T}\right)^3 \le \frac{10}{100}\frac{v_{id}}{2V_T}$$

or $v_{id} \le 2\sqrt{0.3}V_T$

$v_{id} \le 27mV$

- MOSFET

$$i_{DS1} - i_{DS2} = \frac{K_n}{2}\left[(v_{GS1} - V_{TN})^2 - (v_{GS2} - V_{TN})^2\right]$$

But we are interested in the behavior of the transistor in the differential mode

$$v_{GS1} = V_{GS1} + \frac{v_{id}}{2}, \quad v_{GS2} = V_{GS2} - \frac{v_{id}}{2}, \; V_{GS1} = V_{GS2} = V_{GS}, and \; v_{id} = v_1 - v_2$$

$$i_{DS1} - i_{DS2} = \frac{K_n}{2}\left[(V_{GS} - V_{TN} + \frac{v_{id}}{2})^2 - (V_{GS} - V_{TN} - \frac{v_{id}}{2})^2\right]$$

$$= \frac{K_n}{2}\left[(V_{GS} - V_{TN})^2 + (\frac{v_{id}}{2})^2 + (V_{GS} - V_{TN})v_{id} - (V_{GS} - V_{TN})^2 - (\frac{v_{id}}{2})^2 + (V_{GS} - V_{TN})v_{id}\right]$$

$$= K_n (V_{GS} - V_{TN})v_{id}$$

$$\text{Since } I_{DS} = \frac{K_n}{2}(V_{GS} - V_{TN})^2 = K_n (V_{GS} - V_{TN})\frac{(V_{GS} - V_{TN})}{2}$$

$$Hence \; K_n (V_{GS} - V_{TN}) = \frac{2I_{DS}}{V_{GS} - V_{TN}} = g_m$$

$$i_{DS1} - i_{DS2} = K_n (V_{GS} - V_{TN})v_{id} = g_m v_{id}$$

It is clear from this last relationship that, theoretically, there is no constraint on the input for the MOSFET-based differential pair to be considered as a linear system. However, because the MOSFET transistors are not perfect square-law devices, some distortion will still be present because of the dependence of voltages on impedances in the model of the MOSFET transistor.

4) AC Analysis

$$v_{id} = v_1 - v_2$$
$$v_{ic} = (v_1 + v_2)/2$$
$$v_1 = v_{ic} + v_{id}/2$$
$$v_2 = v_{ic} - v_{id}/2$$

- BJT $v_{od} = v_{c1} - v_{c2}$ $v_{oc} = (v_{c1} + v_{c2})/2$
- MOSFET $v_{od} = v_{d1} - v_{d2}$ $v_{oc} = (v_{d1} + v_{d2})/2$

The relationships shown above allow us to think of superposition to obtain the total output due to the common-mode input and the differential-mode input.

$$\begin{pmatrix} v_{od} \\ v_{oc} \end{pmatrix} = \begin{pmatrix} A_{dd} & A_{cd} \\ A_{dc} & A_{cc} \end{pmatrix} \begin{pmatrix} v_{id} \\ v_{ic} \end{pmatrix}$$

$$v_{od} = A_{dd}\, v_{id} + A_{cd}\, v_{ic}$$

$$v_{oc} = A_{dc}\, v_{id} + A_{cc}\, v_{ic}$$

A_{dd} = differential-mode gain

A_{cd} = common-mode to differential-mode conversion gain

A_{cc} = common-mode gain

A_{dc} = differential-mode to common-mode conversion gain

If we assume that we are working with a symmetrical amplifier, then

$A_{cd} = A_{dc} = 0$

Hence

$$\begin{pmatrix} v_{od} \\ v_{oc} \end{pmatrix} = \begin{pmatrix} A_{dd} & 0 \\ 0 & A_{cc} \end{pmatrix} \begin{pmatrix} v_{id} \\ v_{ic} \end{pmatrix}$$

or

$$v_{od} = A_{dd}\, v_{id}$$

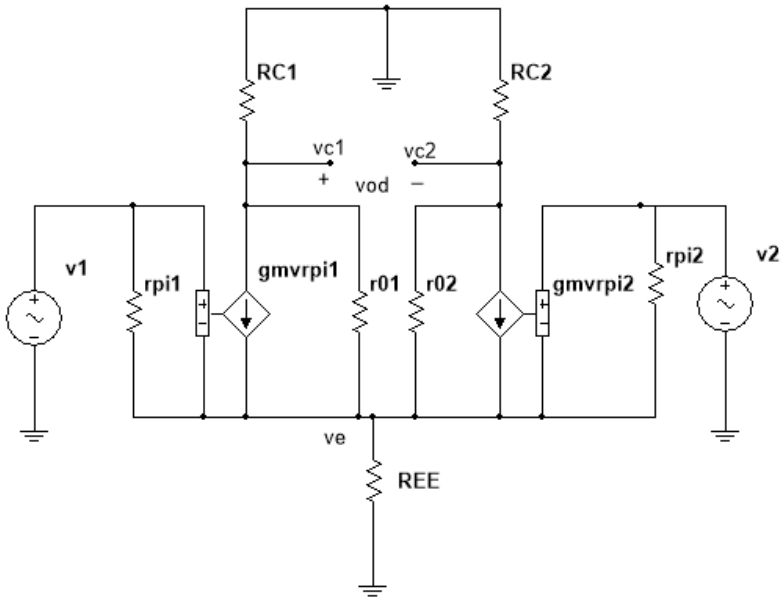
$$v_{oc} = A_{cc}\, v_{ic}$$

a) Differential mode

4.1.1 Differential-Mode Gain

- BJT

The differential-mode equivalent of the differential pair is shown in the figure below.



In this case,

$$R_{C1} = R_{C2} = R_C$$
$$r_{pi1} = r_{pi2} = r_\pi$$
$$r_{01} = r_{02} = r_0$$
$$vr_{pi1} = v_1 - v_e$$
$$vr_{pi2} = v_2 - v_e$$
$$v_1 = v_{id}/2$$
$$v_2 = -v_{id}/2$$
$$v_{c1} = -v_{c2}$$

$$\frac{v_1 - v_e}{r_\pi} + \frac{0 - v_{c1}}{R_C} + \frac{0 - v_{c2}}{R_C} + \frac{v_2 - v_e}{r_\pi} = \frac{v_e}{R_{EE}}$$

$$\frac{v_1 + v_2}{r_\pi} - \frac{v_{c1} + v_{c2}}{R_C} - \frac{2v_e}{r_\pi} = \frac{v_e}{R_{EE}}$$

Note that because of the symmetry, v_{C1} and v_{C2} are equal in magnitude and opposite in sign. Hence, $v_{c1} + v_{c2} = 0$.

In addition, $v_1 + v_2 = \frac{v_{id}}{2} - \frac{v_{id}}{2} = 0$

Hence, $v_e \left(\frac{1}{R_{EE}} + \frac{2}{r_\pi} \right) = 0$

Since both resistances are positive numbers, then

$v_e = 0$

The emitter is virtual ground, and the resistor R_{EE} is a virtual short.

Since v_e is a virtual ground, we see that the two R_{C1} and R_{C2} are in parallel with r_{01} and r_{02}, respectively. In that case,

The current $g_m v_{r_{\pi 1}}$ flows upward in the parallel combination $R_{C1} // r_{01}$

$v_{c1} = -g_m v_{r_{\pi 1}} \; R_{C1} // r_{01}$

but $v_{r_{\pi 1}} = v_{id} / 2$

$v_{c1} = -g_m (R_{C1} // r_{01}) v_{id} / 2$

Similarly

$v_{c2} = g_m (R_{C2} // r_{02}) v_{id} / 2$

Because of symmetry

$v_{c1} = -g_m (R_C // r_0) v_{id} / 2$

$v_{c2} = g_m (R_C // r_0) v_{id} / 2$

$v_{od} = v_{c1} - v_{c2} = -g_m (R_C // r_0) v_{id}$

$A_{dd} = \frac{v_{od}}{v_{id}} = -g_m (R_C // r_0)$

However, in most applications, the subsequent stages have only one input. It would then be practical to extract the output of a differential pair using only one collector.
If the output is at the collector of Q_1, or at the collector of Q_2, then

$$\frac{v_{c1}}{v_{id}} = -\frac{g_m (R_C // r_0)}{2} = -\frac{A_{dd}}{2}$$

$$\frac{v_{c2}}{v_{id}} = \frac{g_m (R_C // r_0)}{2} = \frac{A_{dd}}{2}$$

These last two gains are called single-ended output gains

```
R1=10e3;R2=10e3;R3=47e3;
VBEQ=0.7;beta=136;V1=12;V2=12;VA=74;
IEEQ=(V2-VBEQ)/R3;
IEQ=IEEQ/2;
ICQ=beta/(beta+1)*IEQ;
VCEQ=V1+VBEQ-R2*ICQ;
disp(['The Q-point is ICQ = ',num2str(ICQ*1000),' mA'])
disp(['          VCEQ = ',num2str(VCEQ),' V'])
gm=40*ICQ;r0=(VA+VCEQ)/ICQ;
RL=(1/R1+1/r0)^-1;
Add=-gm*RL;
disp(['The differential-mode gain is equal to ',num2str(Add)])
```

The Q-point is ICQ = 0.11934 mA

VCEQ = 11.5066 V

The differential-mode gain is equal to -47.0771

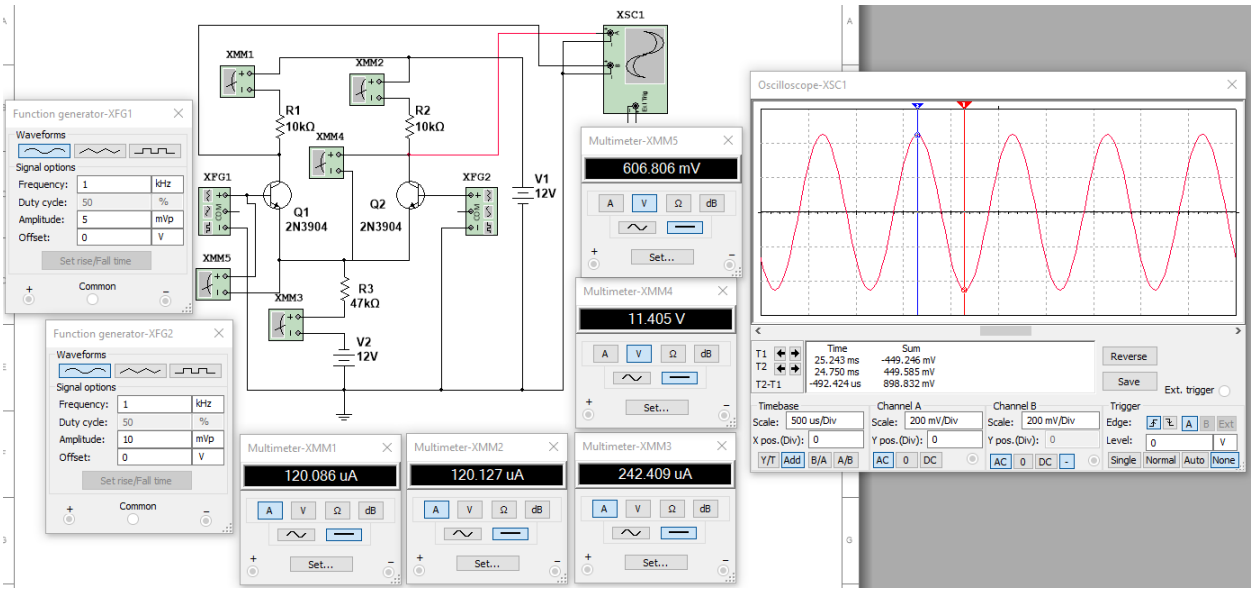
We can see from the Multisim simulation below that the differential-mode gain is evaluated as the ratio of the differential output over the differential input

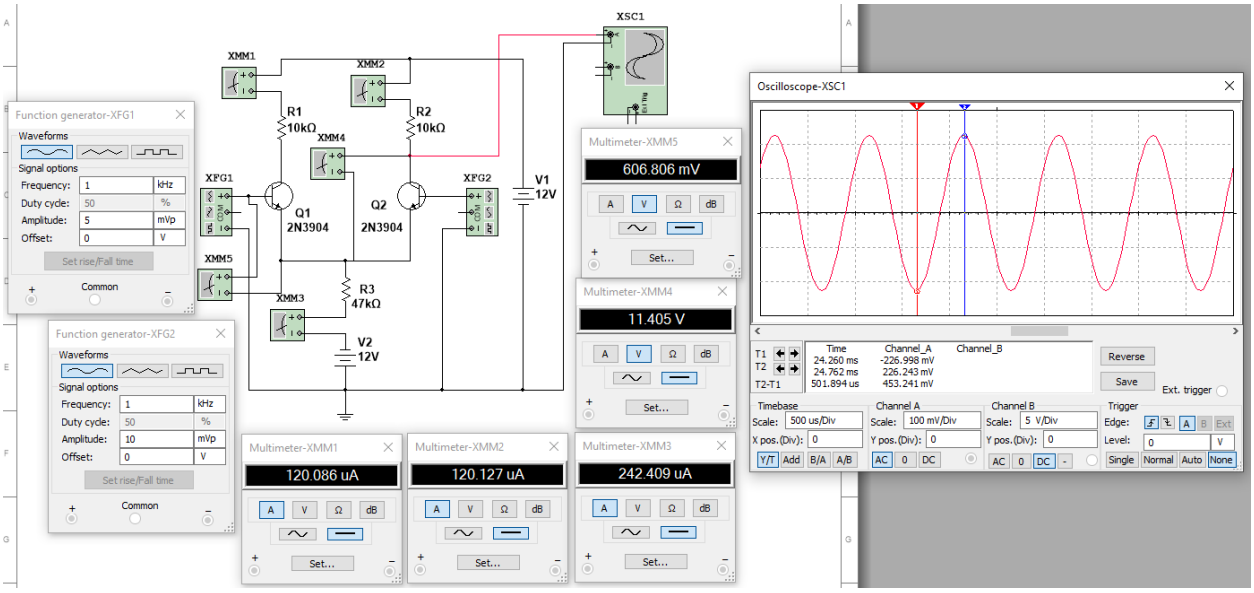
$$A_{dd} = -\frac{449.6}{10} \simeq -45$$

This result is within 4% of the calculated value.

Looking at the single-ended output gain from Multisim

$$A_{dd} = -\frac{227}{10} \simeq -22.7$$





- MOSFET

The analysis will be relegated to the final results because the only difference between a BJT and a MOSFET is that for the MOSFET, $r_\pi = \infty$, $\beta_0 = \infty$, but $\beta_0/r_\pi = g_m$.

```
R1=10e3;R2=10e3;R3=47e3;V1=12;V2=12;Kn=0.1;VTN=2;lambda=1/50;
p=[4*R3^2, -(4*R3*(V2-VTN)+2/Kn),(V2-VTN)^2];
Ids=roots(p);
Vds=V1+V2-(R2+2*R3)*Ids;
Vgs=V2-2*R3*Ids;
%disp(['The two possible values for Ids are      ',num2str(1000*Ids'), ' mA'])
%disp(['The two possible values for Vds are      ',num2str(Vds'), ' V'])
%disp(['The two possible values for Vgs are      ',num2str(Vgs'), ' V'])
for i=1:2
   if Vgs(i)>VTN
      disp(['The Q-point is IDSQ = ',num2str(Ids(i)*1000),' mA'])
      disp(['              VDSQ = ',num2str(Vds(i)),' V'])
      IDSQ=Ids(i);
      VDSQ=Vds(i);
   end
end

gm=sqrt(2*Kn*IDSQ);r0=(1/lambda+VDSQ)/IDSQ;
RL=(1/R1+1/r0)^-1;
Add=-gm*RL/2;
disp(['The single-ended differential-mode gain is equal to ',num2str(Add)])
```

The Q-point is IDSQ = 0.10589 mA

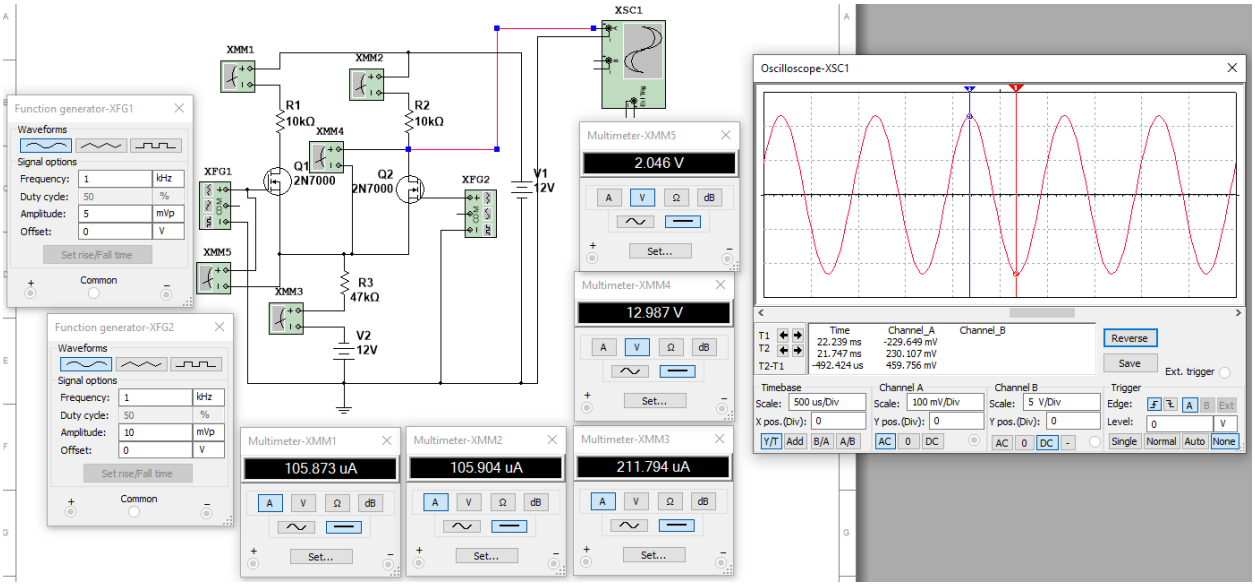
VDSQ = 12.9871 V

The single-ended differential-mode gain is equal to -22.6297

From the Multisim simulation shown below, the single-ended differential-mode gain is equal to:

$$A_{dd} = -\frac{230}{10} \simeq -23$$

This result is within less than 2% of the calculated value



- **Special note about the sign of the gain**

Assume that the differential gain is given by $\frac{v_a - v_b}{v_c - v_d}$

If v_a and v_c are related to the same transistor, then the gain is negative

If v_a and v_c are related to two different transistors, then the gain is positive

4.1.2 Input Resistance

- BJT

Assuming that the current i_{b1} is the current flowing out of the positive terminal of v_1, then we have

$$i_{b1} = \frac{v_1 - v_e}{r_\pi}$$

Assuming that we are interested in the differential mode only

$$v_1 = \frac{v_{id}}{2} \text{ and } v_e = 0$$

$$\text{Hence}, i_{b1} = \frac{\frac{v_{id}}{2}}{r_\pi}$$

$$R_{in} = \frac{v_{id}}{i_{b1}} = 2r_\pi$$

- MOSFET

$R_{in} = \infty$ since $r_\pi = \infty$

4.1.3 Output Resistance

For the differential output

$$R_{od} = 2R_C \,//\, r_0$$

And for single-ended outputs

$$R_{out} = R_C \,//\, r_0$$

4.2 Common Mode

4.2.1 Common-Mode Gain

- BJT

Using the same circuit used in the previous section, but considering that now

$$\mathbf{v_1 = v_2 = v_{ic}}$$

where the differential input is considered to be 0
Remembering the symmetry,

$$\mathbf{v_{c1} = v_{c2} = v_c = v_{oc}}$$

$$\mathbf{i_{b1} = i_{b2} = i_b}$$

$$-v_{ic} + r_\pi i_{b1} + v_e = 0$$

$$R_C\left(\beta_0 i_{b1} + \frac{v_{c1} - v_e}{r_0}\right) + v_{c1} = 0$$

$$v_e = R_{EE}\left(i_{b1} + i_{b2} + \beta_0(i_{b1} + i_{b2}) + \frac{(v_{c1} - v_e) + (v_{c2} - v_e)}{r_0}\right)$$

Since the only interest we have in the common-mode characteristics is that the common-mode gain needs to be as small as possible so that the only output of interest is the output due to the differential input, we are going to simplify a time-consuming calculation by assuming that $r_0 = \infty$.

It is clear that if r_0 were infinite, then

$$A_{cc} = \frac{v_{oc}}{v_{ic}} = -\frac{\beta_0 R_C}{2(\beta_0 + 1)R_{EE} + r_\pi}$$

This relationship is equivalent to the gain of a common-emitter amplifier with an emitter resistor equal to $2R_{EE}$

This relationship could simplify, if $2(\beta_0 + 1)R_{EE} \gg r_\pi$, to

$$A_{cc} = \frac{v_{oc}}{v_{ic}} = -\frac{R_C}{2R_{EE}}$$

One may be led to think from this approximation that if $R_{EE} = \infty$, then

$$A_{cc} = \frac{v_{oc}}{v_{ic}} = 0$$

However, going back to the first expression for the gain if we assume r_0 and R_{EE} to be large but still comparable to each other, and $\beta_0 \gg 1$

$$A_{cc} = \frac{v_{oc}}{v_{ic}} \simeq R_C\left(\frac{1}{\beta_0 r_0} - \frac{1}{2R_{EE}}\right)$$

The approximation may change if we take into account the complete model of the transistor

One can see that the differential-mode conversion gain is 0 since if the inputs are both $v_{id}/2$ and $-v_{id}/2$,, then the output is $v_{oc} = (v_{c1} + v_{c2})/2 = 0$. Conversely, the common-mode conversion gain is 0 since if the inputs are both v_{ic}, then the output is $v_{od} = v_{c1} - v_{c2} = 0$.

- MOSFET

In this case, let $\beta_0 = \infty$, $r_\pi = \infty$, $\beta_0 / r_\pi = g_m$

It is clear that if r_0 were infinite, then

$$A_{cc} = \frac{v_{oc}}{v_{ic}} = -\frac{g_m R_D}{1 + 2 g_m R_{SS}}$$

which, if $2 g_m R_{SS} \gg 1$, reduces to

$$A_{cc} = \frac{v_{oc}}{v_{ic}} \simeq -\frac{R_D}{2 R_{SS}}$$

However, going back to the first expression for the gain, if we assume r_0 and R_{SS} to be large but still comparable to each other, and $R_D = r_0$, The approximation above is still valid considering the infinite current gain of the MOSFET
The approximation may change if we take into account the complete model of the transistor

1) Input Resistance

A] Common-mode input resistance

- BJT

$$R_{ic} = \frac{v_{ic}}{2 i_b} = \frac{r_\pi i_b + R_{EE}(2\beta_0 i_b + 2 i_b)}{2 i_b}$$

$$R_{ic} = \frac{r_\pi}{2} + (\beta_0 + 1) R_{EE}$$

- MOSFET

$R_{ic} = \infty$

5) Common-Mode Rejection Ratio (CMRR)

This parameter shows the ability of the differential amplifier to render the output signal more dependent of the differential-mode input rather than the common-mode input, and hence desired to be as large as possible.

- BJT

A balanced amplifier is assumed to have an infinite CMRR. However, for a single-ended output amplifier,

$$CMRR = \left|\frac{A_{dm}}{A_{cm}}\right| = \left|\frac{A_{dd}/2}{A_{cc}}\right| = \left|\frac{1}{2\left(\frac{1}{\beta_0\mu_f} - \frac{1}{2g_m R_{EE}}\right)}\right|$$

Hence, even if we were able to have $R_{EE} = \infty$, the CMRR is still limited by $\beta_0\mu_f$

- MOSFET

$$CMRR = \left|\frac{A_{dm}}{A_{cm}}\right| = \left|\frac{A_{dd}/2}{A_{cc}}\right| = g_m R_{SS}$$

This is easily obtained from the BJT model replacing β_0 with infinity

A resistive biasing is not practical because a large R_{EE} or R_{SS} would lead to very low biasing currents, or requiring extremely large power supplies.
As an example, let us assume that we require I_{EE} or I_{SS} to be 1 mA. If R_{EE} or R_{SS} were to be 1 MΩ, then neglecting the potential at the common emitter or the common source,

$$V_{EE} = R_{EE} I_{EE} = 10^6 * 10^{-3} = 1000V$$

or

$$V_{SS} = R_{SS} I_{SS} = 10^6 * 10^{-3} = 1000V$$

This DC power supply is definitely not practical for this implementation