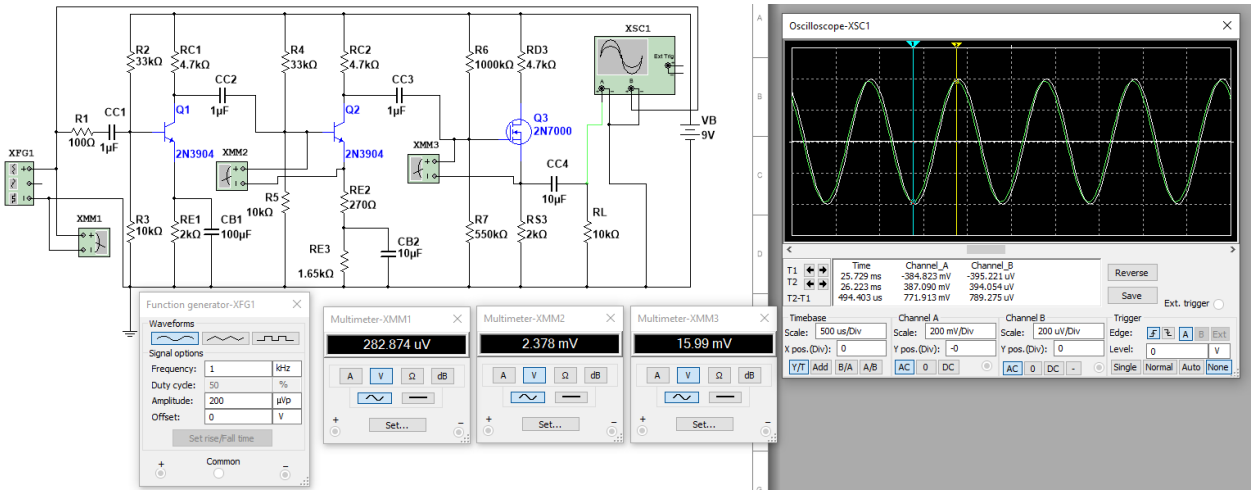
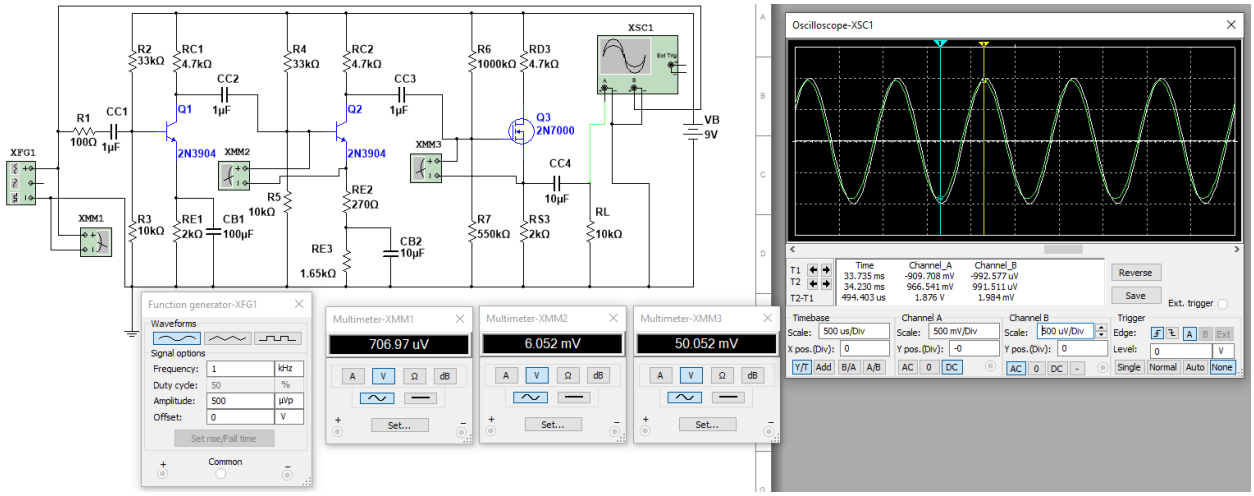
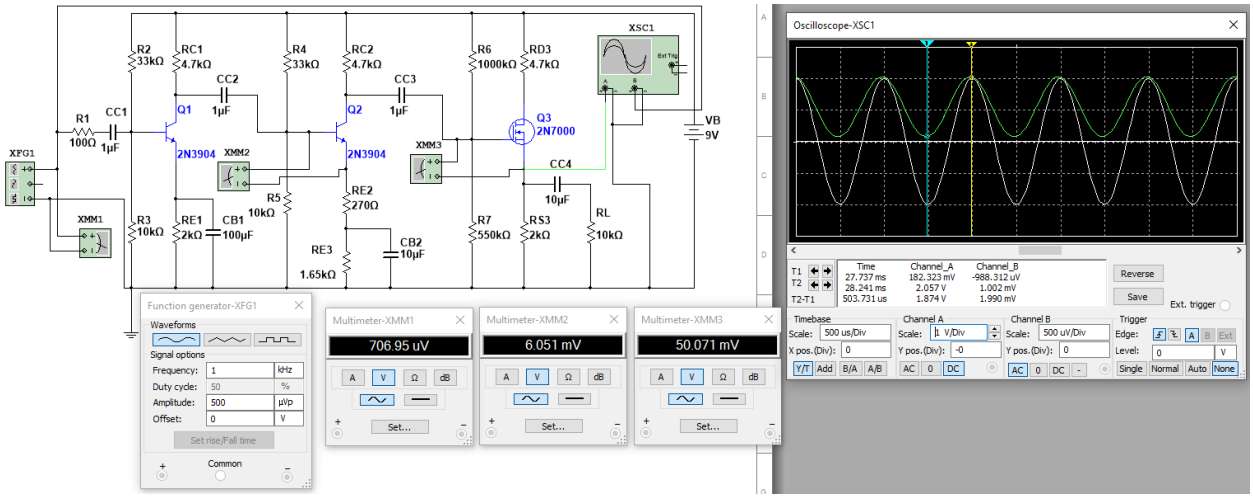
Chapter 4

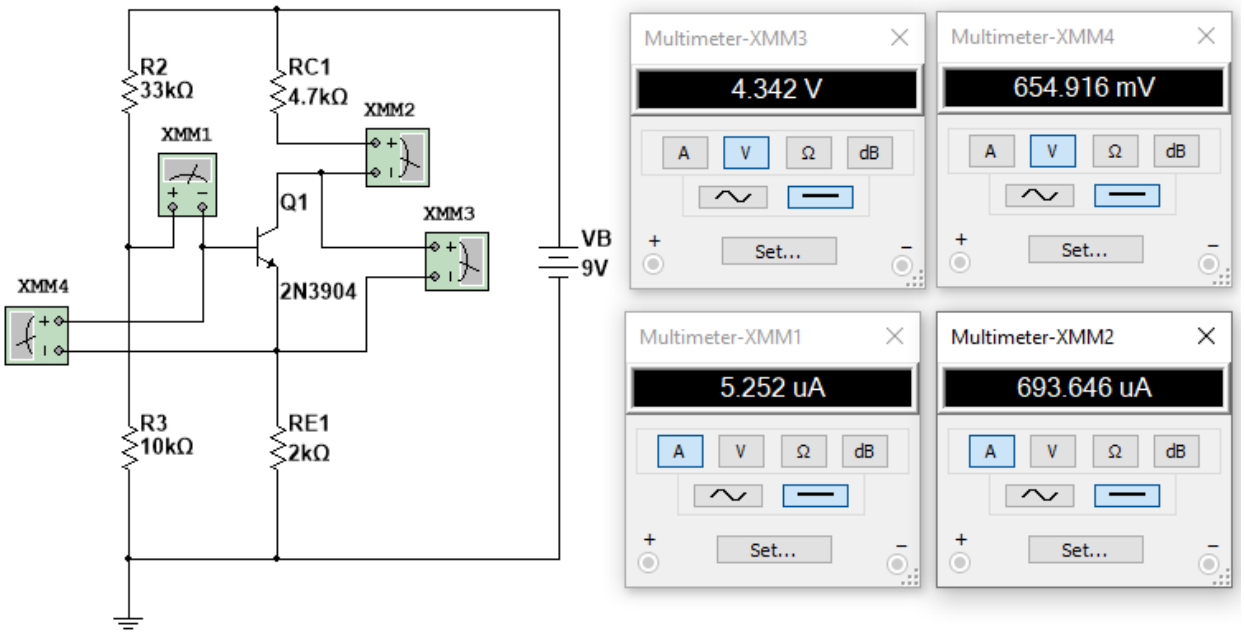
Multistage Amplifier

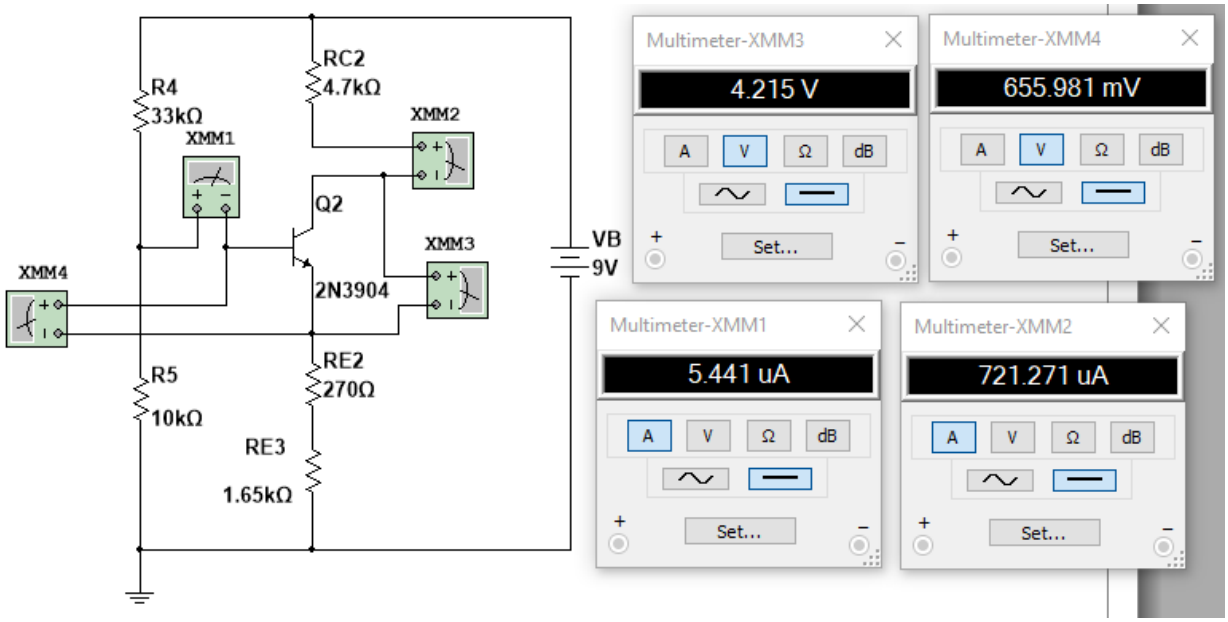
1. DC Equivalent and Analysis of a Multistage Amplifier

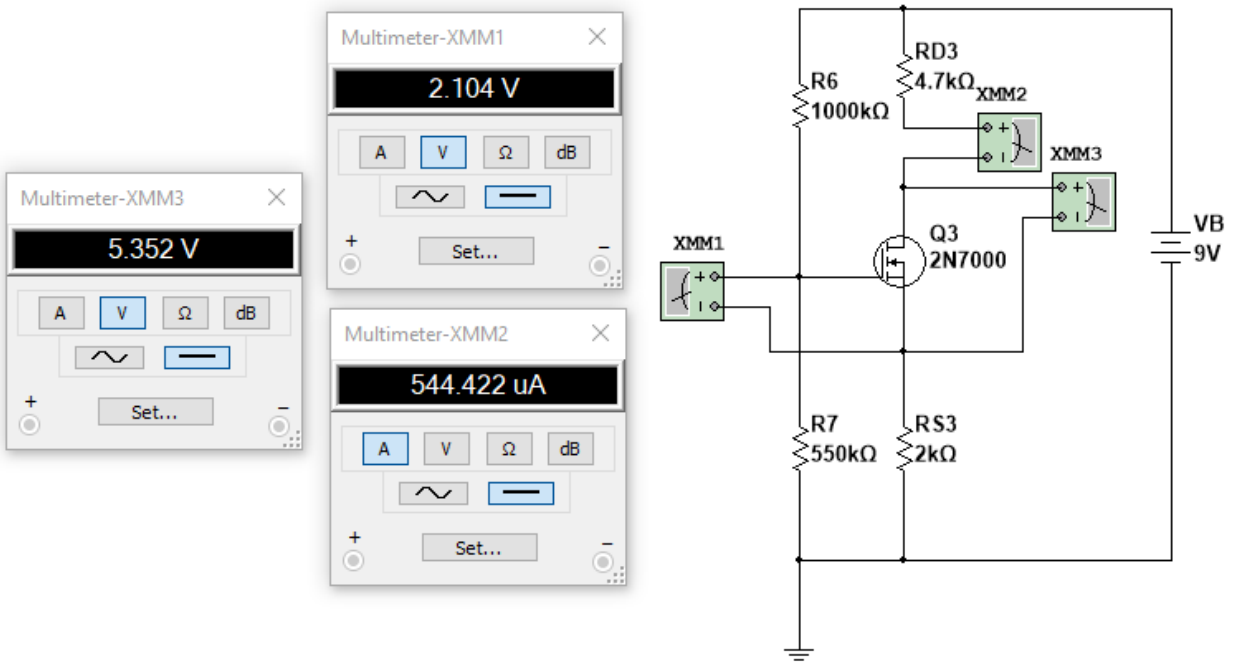





R2
33kΩ
RC1
4.7kΩ
R4
33kΩ
RC2
4.7kΩ
R6
1000kΩ
RD3
4.7kΩ
XSC1
CC2
1µF
CC3
1µF
R1
100Ω
CC1
1µF
Q1
2N3904
Q2
2N3904
Q3
2N7000
VB
9V
XFG1
XMM2
XMM3
CC4
10µF
R5
10kΩ
RE2
270Ω
XMM1
R3
10kΩ
RE1
2kΩ
CB1
100µF
RE3
1.65kΩ
CB2
10µF
R7
550kΩ
RS3
2kΩ
RL
10kΩ
Oscilloscope-XSC1
Function generator-XFG1
Waveforms
Signal options
Frequency:
Duty cycle:
Amplitude:
Offset:
Set rise/Fall time
Common
Multimeter-XMM1
706.95 uV
Multimeter-XMM2
6.051 mV
Multimeter-XMM3
50.071 mV
Set...
Time
Channel_A
Channel_B
Reverse
Save
Ext. trigger
Timebase
Channel A
Channel B
Trigger
Scale:
X pos.(Div):
Y pos.(Div):
Edge:
Level:
Add
B/A
A/B
AC
DC
Single
Normal
Auto
None


R2
33kΩ
RC1
4.7kΩ
XMM2
XMM1
Q1
XMM3
VB
9V
XMM4
2N3904
R3
10kΩ
RE1
2kΩ
Multimeter-XMM3
4.342 V
Multimeter-XMM4
654.916 mV
Multimeter-XMM1
5.252 uA
Multimeter-XMM2
693.646 uA
A
V
Ω
dB
Set...





It is clear that this multistage amplifier is made of three stages, a BJT-based common-emitter amplifier, a BJT-based common-emitter amplifier with emitter degeneration, and an enhanced NMOS common-drain amplifier.

```
R1=100;R2=33e3;R3=10e3;R4=33e3;R5=10e3;R6=1000e3;R7=550e3;
RC1=4.7e3;RE1=2e3;RC2=4.7e3;RE2=270;RE3=1.65e3;beta=136;VBEQ=0.65;
RD3=4.7e3;RS3=2e3;RL=10e3;VA=74.03;VTN3=2;Kn3=0.1;lambda=1/50;
```

```
RB1=1/(1/R2+1/R3);RB2=1/(1/R4+1/R5);RG3=1/(1/R6+1/R7);
VB=9;VBB1=R3/(R2+R3)*VB;VBB2=R5/(R4+R5)*VB;VG3=R7/(R6+R7)*VB;

A1=[RB1/beta+RE1,0;RC1+RE1,1];
B1=[VBB1-VBEQ;VB];
IVcq1=A1\B1;
disp(['The Q-point for the 1st stage is ICQ1 = ',num2str(IVcq1(1)*1000),' mA'])
disp(['                                    VCEQ1 = ',num2str(IVcq1(2)),' V'])
ICQ1=IVcq1(1);VCEQ1=IVcq1(2);
gm1=40*ICQ1; rpi1=beta/gm1; r01=(VA+VCEQ1)/ICQ1;
Ric1=r01;Roc1=1/(1/RC1+1/r01);

A2=[RB2/beta+(RE2+RE3),0;RC2+(RE2+RE3),1];
B2=[VBB2-VBEQ;VB];
IVcq2=A2\B2;
disp(['The Q-point for the 2nd stage is ICQ2 = ',num2str(IVcq2(1)*1000),' mA'])
disp(['                                     VCEQ2 = ',num2str(IVcq2(2)),' V'])
ICQ2=IVcq2(1);VCEQ2=IVcq2(2);
gm2=40*ICQ2; rpi2=beta/gm2; r02=(VA+VCEQ2)/ICQ2;
Rth2=1/(1/Roc1+1/RB1);
Ric2=r02*(1+beta*RE2/(Rth2+rpi2+RE2));

Rinb1=1/(1/RB1+1/rpi1);
RLC2=1/(1/RG3+1/RC2);
Rinb2=rpi2+RE2*(1+(beta*r02-RE2)/(RLC2+r02+RE2));
RLC1=1/(1/Rinb2+1/Roc1+1/1/RB2);

p=[RS3^2, -(2*(VG3-VTN3)*RS3+2/Kn3),(VG3-VTN3)^2];
Ids=roots(p);
Vds=VB-(RD3+RS3)*Ids;
Vgs=VG3-RS3*Ids;
```

```
for i=1:2
   if Vgs(i)>VTN3
      IDSQ=Ids(i);VDSQ=Vds(i);
      disp(['The Q-point for the 3rd stage is IDSQ = ',num2str(Ids(i)*1000),' mA'])
      disp(['                                    VDSQ = ',num2str(Vds(i)),' V'])
   end
end

gm3=sqrt(2*Kn3*IDSQ); r03=(1/lambda+VDSQ)/IDSQ;
Rid=r03*(1+gm3*RS3);RLS0=1/(1/RS3+1/r03+1/RL);

Gain1=-RLC1*(beta*r01)/((RLC1+r01)*(rpi1));
Gain2=-RLC2*(beta*r02-RE2)/((RLC2+r02+RE2)*(rpi2+RE2)+RE2*(beta*r02-RE2));
Gain3=gm3*RLS0/(1+gm3*RLS0);
Gain=Rinb1/(R1+Rinb1)*Gain1*Gain2*Gain3;
%Rin=R1+1/(1/Rinb1+1/RB);

disp(['The voltage gain for the 1st stage is ',num2str(Gain1)])
disp(['The voltage gain for the 2nd stage is ',num2str(Gain2)])
disp(['The voltage gain for the 3rd stage is ',num2str(Gain3)])
disp(['The voltage gain for the 3 stages is ',num2str(Gain1*Gain2*Gain3)])
disp(['The voltage gain v0/vin for the 3-stage amplifier is ',num2str(Gain)])

%disp(['The input resistance is ',num2str(Rin/1000),' kOhms'])
%disp(['The output resistance seen from the collector is ',num2str(Ric/1e6),' MOhms'])
%disp(['The output resistance seen by RL is ',num2str(Rout/1000),' kOhms'])
```

The Q-point for the 1st stage is ICQ1 = 0.70171 mA

VCEQ1 = 4.2985 V

The Q-point for the 2nd stage is ICQ2 = 0.73012 mA

VCEQ2 = 4.1666 V

The Q-point for the 3rd stage is IDSQ = 0.54459 mA

VDSQ = 5.3512 V

The voltage gain for the 1st stage is -72.7233

The voltage gain for the 2nd stage is -15.0658

The voltage gain for the 3rd stage is 0.94479

The voltage gain for the 3 stages is 1035.1452

The voltage gain v0/vin for the 3-stage amplifier is 1001.4282

Let us study each stage separately.

1.1 First stage

Since the first stage is a BJT-based common-emitter amplifier, the voltage gain v_{c1}/v_{b1} is equal to:

$$Gain1 = -\frac{R_{LC1}(\beta_0 * r_{01})}{(R_{LC1} + r_{01})\, r_{\pi 1}}, \text{ where}$$

$$R_{LC1} = R_{inb2} // R_{oc1} // R_{B2}$$

$$R_{B2} = R_2 // R_3$$

$$R_{oc1} = R_{C1} // r_{01}$$

$$R_{inb2} = r_{\pi 2} + R_{E2}\left(1 + \frac{\beta_0 * r_{02} - R_{E2}}{R_{LC2} + r_{02} + R_{E2}}\right)$$

1.2 Second stage

The second stage is also a BJT-based common-emitter amplifier with emitter degeneration; hence, the voltage gain v_{c2}/v_{b2} is equal to:

$$Gain2 = -R_{LC2}\,\frac{(\beta_0 * r_{02} - R_{E2})}{(R_{LC2} + r_{02} + R_{E2})(r_{\pi 2} + R_{E2}) + R_{E2}(\beta_0 * r_{02} - R_{E2})}$$

where

$$R_{LC2} = R_{C2} // R_{G3}$$

$$R_{G3} = R_6 // R_7$$

1.3 Third stage

The third stage is an enhanced-NMOS-based common-drain stage; hence, the voltage gain v_0/v_{g3} is equal to:

$$Gain3 = \frac{gm_3 R_{LS0}}{1 + gm_3 R_{LS0}}$$

where

$$R_{LS0} = R_L \,//\, R_{S3} \,//\, r_{03}$$

1.4 Total gain

The voltage gain of this 3-stage voltage amplifier v_0/v_{in} is equal to:

$$\frac{v_0}{v_{in}} = \frac{R_{inb1}}{R_1 + R_{inb1}} Gain1\, Gain2\, Gain3$$

The calculated values are closely related to the values obtained through Multisim (a gain of approximately 771.913/(789.275 10^{-3}) or 978). The gain does not vary greatly when we increased the input to a 1mV-peak sinewave from a 400μV-peak sinewave, when the gain was about 945.6. The decrease in the gain can be seen through the distortion that is somehow visible in the output signal (flatter peak). One can see that the base-emitter junction of the second stage has exceeded the minimum suggested for linearity. In addition, in the third figure, we note that the output signal would be riding a DC level if it were not for the output coupling capacitor. The level was not high enough to allow the sinewave to be larger without getting dangerously close to the rail. Of course, in designing this amplifier, the engineer will take into account all that is required and will tweak the component values until satisfaction is obtained.

In addition, we sometimes may be justified in using approximations when justified, as had been done in some of these calculations. We could have easily evaluated many of the transistors' parameters or the amplifier characteristics through additional approximations. We let the user compare the values obtained through the exact expressions and experiment with additional approximations, and learn to decide when the approximations are justified.

We will evaluate in the next section the input and the output resistances of this amplifier.

1.5 Input resistance

The input resistance seen by v_{in} is obtained as the series connection of R_1 and the input resistance of the first stage R_{inb} given by $R_B//r_{\pi 1}$

$R_{in} = R_1 + R_B// \, r_{\pi 1}$

1.6 Output resistance

The output resistance seen by R_L is simply given by $R_{S3}//1/g_{m3}$

$R_{out} = R_{S3}//1/g_{m3}$