DIGITAL UTILITY SUB-SYSTEMS

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ACHIEVEMENTS: *an awareness of various sub-systems included within modules to which independent access may be made.*

PREREQUISITES: *none.*

ADVANCED MODULES: *various ! See below.*

INTRODUCTION

Many modules in the *Advanced Modules* set have sub-systems within them to help them perform their main function. Many of these modules allow direct access to these sub-systems. So they may be used independently in other models.

It is often forgotten that these sub-systems are available. This chapter serves as a reminder of their existence, and gives brief details of their properties.

bandpass filters

There are two identical but independent analog bandpass filters, BPF1 and BPF2, built into the BIT CLOCK REGEN module.

They are order 4 Chebyshev bandpass filters. They have mid-band gains of unity.

A clock signal to each filter may be supplied internally or externally (to the *EXT CLK* socket), as determined by an on-board switch SW1.

- when the **int**ernal clock is selected the response is centred on 2.083 kHz, with -3 dB bandwidths of about 100 Hz, and -40 dB bandwidths of about 700 Hz.
- when an **ext**ernal TTL clock is selected the centre frequency may be tuned over the range 1 kHz to 5 kHz. The clock frequency should be 50 times the desired centre frequency.

The clock source selections are made with SW1, according to the settings given in the Table below.

SW1-1	SW1-2	BPF1 clock	BPF2 clock
DOWN	DOWN	EXT	EXT
DOWN	UP	EXT	INT
UP	DOWN	INT	EXT
UP	UP	INT	INT

BPF operation in terms of clock source

There is only one EXT CLK input provided. Thus, when BPF1 and BPF2 both have external clock selected by SW1, they both receive the same clock.

reminder: the 2.083 kHz (which is 1/48 of the TIMS 100 kHz MASTER CLOCK), is a common bit rate for many experiments.

digital delay

This sub-system is built into the INTEGRATE & DUMP module.

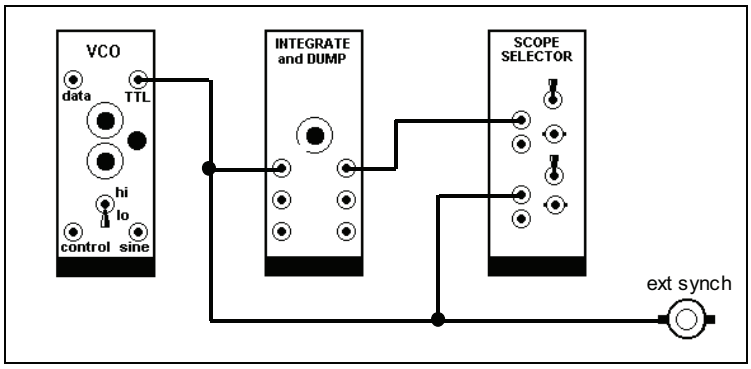
The input is a TTL clock signal. The output is a train of pulses of the same repetition rate, but of width about 10 µsec (fixed). The operating frequency of the clock should be below 15 kHz.

The delay is adjustable by a front panel control DELAY, in conjunction with a toggle switch SW3 mounted on the circuit board. The delays to be expected are shown in the table below.

SW3-upper toggle	*SW3-lower toggle*	*delay range from front panel, using DELAY*
RIGHT	RIGHT	10 µsec - 100 µsec
RIGHT	LEFT	60 µsec - 500 µsec
LEFT	RIGHT	100 µsec - 1 msec
LEFT	LEFT	150 µsec - 1.500 msec

on-board switch SW3 settings

You can check the delay between the input and output TTL pulseforms by a scheme such as shown in the Figure below.



demonstration of digital delay

The display on CH1-A will be of the input TTL clock, obtained from a VCO in the LO frequency range.

The display on CH2-A will be a train of 10µsec wide pulses, synchronized to the input clock. The relative position of these two TTL pulse trains may be varied with the front panel control of the INTEGRATE & DUMP module (in conjunction with the switch settings shown in the Table above).

digital divide-by-1, 2, 4, or 8

This sub-system is built into the BIT CLOCK REGEN module.

The frequency of the input TTL signal must be held below 15 kHz.

Division by a factor of 1, 2, 4, and 8 are selected by the on-board switch SW2, according to the scheme of the Table below.

Note that the 'divide by 1' option introduces an inversion.

SW2-A (left)	*SW2-B (right)*	*divide by*
DOWN	DOWN	8
DOWN	UP	4
UP	DOWN	2
UP	UP	-1

switch selectable division ratios

digital divide-by-2, 3, 4

The DIGITAL UTILITIES module has two each of TTL divide-by-2, divide-by-3, and divide-by 4 sub-systems.

It also has a TTL divide-by-minus 1, which offers a polarity inversion.

digital divide-by-4

This sub-system is built into the LINE-CODE ENCODER module.

The input must be TTL, as is the output. The output has a mark-space ratio of 1:1.

Accepts TTL signals anywhere within the TIMS range - from 100 kHz down.

digital divide-by-8

This sub-system is built into the CONVOLUT`L ENCODER module.

The input must be TTL, as is the output. The output has a mark-space ratio of 1:1 for any mark-space ratio of the input.

Accepts TTL signals anywhere within the TIMS range - from 100 kHz down.

digital inversion

This is available in the DIGITAL UTILITIES module.

exclusive-or

This sub-system is built into the ERROR COUNTING UTILITIES module.

It accepts two TTL input signals whose logical X-OR (EXCLUSIVE-OR) sum is required. The output depends on which of the two available modes is in use.

gated mode

Requires a TTL clock. The logic result is computed and presented at the output only during the HI of the clock pulse. For precise timing details it is best to make some measurements on the logic operation under the conditions in which you are interested ! When used in company with the pulse counting facility (a second sub-system within the module) these details are taken care of automatically.

normal mode

If no clock signal is provided, then the output is a continuous result of the X-OR operation.

frequency doubler

There is a transition detector in the BIT CLOCK REGEN module. It is optimised to work in the region of 2 kHz. For an input TTL signal it gives an adjustable width TTL output pulse for every input logic transition.

Thus, for a rectangular input at 2 kHz the output is rectangular at 4 kHz.

The width of the output pulse can be adjusted with the on-board variable resistor RV1 -VARY PULSE WIDTH - provided the jumper J1 is in the VARY position..

integrate and dump

Two identical integrate-and-dump (I&D) sub-systems are built into the INTEGRATE & DUMP module.

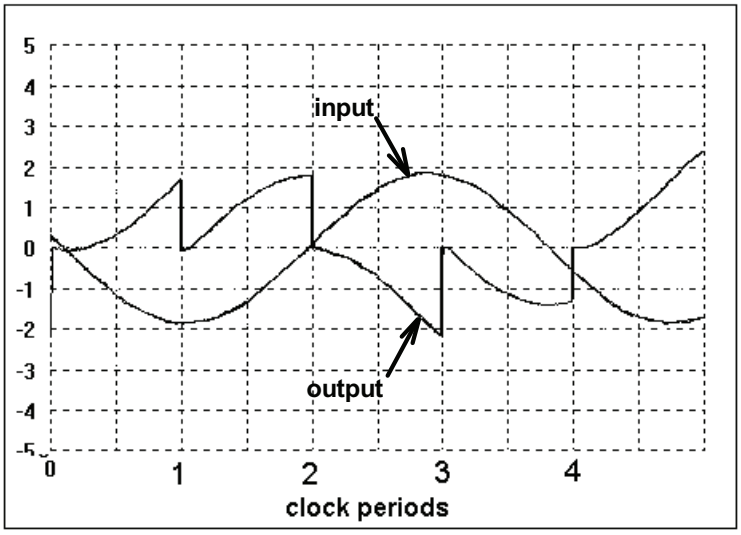
Each sub-system is driven by the same TTL clock, at a rate less than 15 kHz.

The input to each sub-system is an analog waveform.

Although the sub-system inputs and outputs are labelled I&D 1 and I&D 2 (they identify with the name of the module), they represent the input and output sockets of sub-system #1 and sub-system #2. The integrate and dump operation is obtained with on-board rotary switches SW1 and SW2 respectively (position '5').

The integration starts after a small delay, on the rising edge of the clock pulse. It is continuously available at the output until the end of the clock pulse, when it is dumped and a new integration period commences. *Note that the integrator inverts.*

This is illustrated in the Figure below.



integrate and dump of a sine wave (the integrator inverts)

The time constants of the integrators are:

integrator	*R*	*C*	*comments*
1	R7 = 330 kohm	C4 = 470 pF	fixed
2 - option 1	R26 = 330 kohm	C34 = 470 pF	J1 open
2 - option 2	R26 = 330 kohm	C34+C44 = 940 pF (jumper at 'IN')	J1 shorted adds C44 to C34

The jumper J1 is on the circuit board.

integrate and hold

Two identical integrate-and-hold sub-systems are built into the INTEGRATE & DUMP module.

Each sub-system is driven by the same TTL clock, at a rate less than 15 kHz.

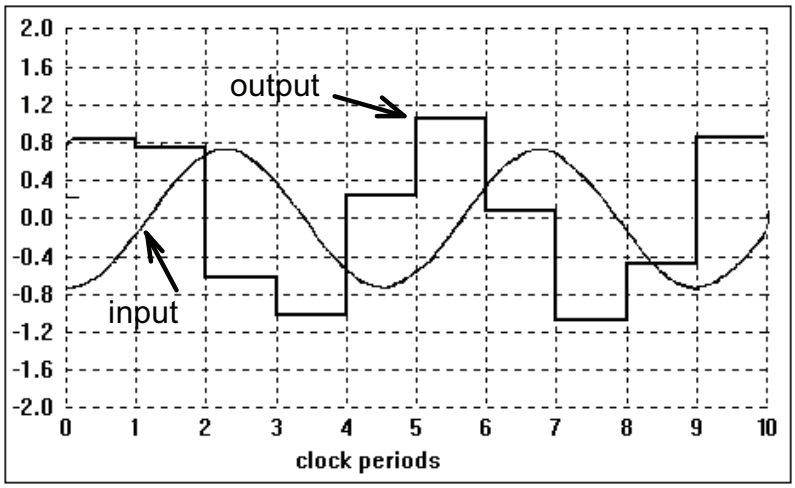
The input to each sub-system is an analog waveform.

Although the sub-system inputs and outputs are labelled I&D 1 and I&D 2 (they identify with the name of the module), they represent the input and output sockets of sub-system #1 and sub-system #2. The integrate and hold (I&H) operation is obtained with on-board rotary switches SW1 and SW2 respectively (position '2' or '3').

operation: the input is integrated over the period of the clock. Integration commences at a rising edge of the clock pulse, and ceases at the next rising edge. At the end of the period the result is presented at the output, and held there for the next clock period. At the same time the integrator is re-set, and the cycle is repeated.

A pulse of fixed width (about 10 μs) at the READY output occurs some time after the rising edge of the clock, to indicate that the output has been updated and has settled.

See the Figure below, for the case of a sinusoidal input, synchronous with the clock. This is the sort of display you can observe if you use the 2 kHz MESSAGE and the 8.333 kHz SAMPLE CLOCK signals from the MASTER SIGNALS module for the input and clock respectively. *Note that the integrator inverts.*



integrate and hold of a sine wave (the integrator inverts)

The time constants of the integrators are:

integrator	*R*	*C*	*comments*
1	R7 = 330 kohm	C4 = 470 pF	fixed
2 - option 1	R26 = 330 kohm	C34 = 470 pF	J1 open
2 - option 2	R26 = 330 kohm	C34+C44 = 940 pF (jumper at 'IN')	J1 shorted adds C44 to C34

The jumper J1 is on the circuit board.

limiter - 1

This sub-system is built into the DELTA MODULATION UTILITIES module.

It accepts analog input (it will saturate with inputs in excess of the TIMS ANALOG REFERENCE LEVEL of ±2 V).

The output is a TTL HI for inputs above 10 mV, and a TTL low otherwise.

This is a COMPARATOR, with respect to 10 mV. It makes a convenient 'analog-to-TTL converter' (eg, sine to TTL).

limiter - 2

There are two hard limiters in the FM UTILITIES module.

limiter - 3

This is part of the (analog) UTILITIES module. It may be set to soft limit as well.

pulse width modulator - PWM

This sub-system is built into the INTEGRATE & DUMP module. It is the subject of the experiment entitled *PWM and PPM* (in this Volume).

sample and hold

This sub-system is built into the INTEGRATE & DUMP module. It is the subject of the experiment entitled *Sampling with sample and hold* (in volume D1).

square TTL - 20 to 200 kHz

It is not always realised that the VCO can provide a TTL square wave anywhere in the range 500 Hz to 200 kHz. This is in the FSK mode.

By connecting either a TTL LO or a TTL HI to the DATA input socket, the output is either f_1 or f_2. The range of f_1 is changed with the on-board control RV7, and f_2 with RV8. Together with the front panel HI/LO toggle switch the VCO output (in FSK mode) can cover the range from below 500 Hz to well over 200 kHz.

An sinusoidal output is available simultaneously.

timed pulse

This sub-system is built into the ERROR COUNTING UTILITIES module.

The sub-system is driven by a TTL clock, from which it derives timing information.

default mode

On receipt of a momentary TTL HI at the TRIGGER input, or a push of the PUSH BUTTON, a TTL LO appears at the GATE output socket. It is otherwise HI.

This GATE LO remains for a preset number of clock cycles (10^3, 10^4, 10^5, or 10^6) as determined by the front panel four-position switch PULSE COUNT. But see 'gate time multiplier' below.

other modes

The above description of the TRIGGER and GATE pulses is what might be called the default mode. But an on-board toggle switch SW1 enables either or both of these states to be reversed.

usage

A typical usage is in an error counting situation, where the GATE pulse is used to initiate a counting operation. Hence the sub-system is part of the ERROR COUNTING UTILITIES module.

gate time multiplier

The front panel rotary switch indicates the number of clock cycles for which the GATE is open. But these can be altered by an on-board double pole switch SW2 and a jumper J1.

- ***normal mode:*** jumper J1 in norm position. Front panel multiplier is x1.
- ***extended mode*** jumper J1 in norm position. SW2 according to details written on the circuit board. Multipliers of x1 (default), x2, x4, and x8 are available.
- ***expanded mode*** jumper J1 in ÷12 position.. See the *TIMS Advanced Modules User Manual* for more details. This mode is applicable when using a 100 kHz bit rate.

TTL HI

Available from the DIGITAL UTILITIES and VARIABLE DC modules.

transition detector

This sub-system is built into the BIT CLOCK REGEN module.

It accepts as input any TTL signal likely to be found in the TIMS environment.

Its output is a positive TTL pulse for each transition (ie, in either direction) of the input.

The pulse width may be adjusted with the on-board VARY PULSE WIDTH variable resistor RV (with the on-board jumper J1 in the VARY position). To avoid anomalous operation the width must be less than that of the period of the bit clock.

The module has been optimized for operation at a bit clock of 2.083 kHz. This mode is selected with the on-board jumper J1 in the FIX position. In this case the pulse width is fixed at about half the period of the bit clock.

unit delay

An INTEGRATE & HOLD sub-system is available in the INTEGRATE & DUMP module.

This is a clocked sub-system.

When fed with a train of pulses, synchronous with the clock, this train is output one clock period later. A property of this particular sub-system is that the output is inverted in polarity.